REMARKS

Claims 1-13 stand rejected under 35 U.S.C. § 112, second paragraph. This rejection is respectfully traversed for the following reasons.

In order to expedite prosecution, Applicants' representative initiated a telephone interview with Examiner Crane. Applicants and Applicants' representative would like to thank Examiner Crane for her courtesy in conducting the interview and for her assistance in resolving issues. During the interview, Applicants' representative explained why the claims, as currently recited, are definite and distinguish over the cited prior art. Examiner Crane indicated that reconsideration of the pending rejections would be made upon receiving a formal response. A summary of the interview discussion follows.

In the outstanding Office Action, the Examiner asks whether there is a structural difference between the recited "actually used" transistor and the "MIS transistors used for evaluation." As noted by the Examiner, one exemplary embodiment of the present invention can embody an "actually used" transistor and "MIS transistors used for evaluation" having substantially the same structure (e.g., claim 7). In this regard, the respective transistors can have, in one exemplary embodiment, "their gate electrodes, gate insulating films, source and drain regions, and other configurations [be] substantially the same" (*see* page 8, lines 11-12 of Applicants' specification). As described in Applicants' specification, such similarity can enable the measured characteristics by the evaluation transistors to more accurately reflect those of the actually used transistors.

However, it is respectfully submitted that one of ordinary skill in the art would recognize the structural differences between an "actually used" transistor and "MIS transistors used for evaluation" *in relation to the connections adapted therefor*. For example, with respect to an

evaluation transistor, a terminal such as a voltage-applying terminal and a current-measuring terminal would be adapted to contact the source pad 12, the drain pad 13, and the gate pad 14, so that the electric characteristics such as I-V characteristics can be evaluated whereby the evaluation results can be stored in a memory (*see* page 9, lines 5-8 of Applicants' specification corresponding to Figure 1, for example).

Whereas, an "actually used" transistor's interconnections would be related to the operation of the semiconductor integrated circuit itself so as to not be adapted for connecting to any such measurement terminal, etc.. In view of the interfaces related to the differing connections for which the respective transistors are adapted, it is respectfully submitted that one of ordinary skill in the art would recognize the meaning of an "actually used" transistor and "MIS transistors used for evaluation" so as to render those terms definite within the meaning of 35 U.S.C. § 112, second paragraph.

The Examiner further inquires about the meaning of the term "dummy active regions." As discussed during the interview, it is respectfully submitted that the term "active region" in the above-recitation is merely used as a *title* to identify the semiconductor section being referenced as the "dummy" section, rather than used to imply that the region is actually active. An "active region" *per se* is well-known in the art, and a dummy active region simply corresponds to a conventional active region *in relation to, for example, shape and configuration*, etc; but a dummy active region does not function as a conventional active region.

Although no prior art rejection was made, the Examiner implies that Chen et al. may be relevant to the claimed invention. However, in view of the clarification above, it is clear that Chen et al. does not disclose or suggest the combination of features recited in the pending claims. Specifically, Chen et al. is related only to evaluation transistors which determine dopant

distribution or uniformity of the impurity diffusion layer in the ion implantation process and is unrelated to, for example, typifying characteristics of an "actually used" transistor. In this regard, as set forth in the claimed combination, the present invention embodies a semiconductor substrate including both an "actually used" transistor and "MIS transistors used for evaluation," rather than just evaluation transistors. Based on the foregoing, it is respectfully submitted that claims 1-13 are definite and patentable over the cited prior art. Accordingly, it is respectfully requested that the rejection under 35 U.S.C. § 112, second paragraph be withdrawn.

CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below. To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,
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